Shahzaib Kashif

Software Engineer

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EXPERIENCE

Microelectronics Research Lab (MERL) — *Research Assistant*

September 2022 - Present (7 months+)

Intensivate, Berkeley — *RISC-V CPU Logic Implementor (CHISEL)*

October 2022 - Present (6 months+)

Microelectronics Research Lab (MERL) — *Research Intern*

September 2019 - September - 2022 (3 years)

EDUCATION

Usman Institute of Technology — *BSc*

2018 - 2022

Bachelor of Science (BSc), Software Engineering.

PROJECTS

MAGMA-Si — *A Network on Chip (NoC) based Generic Matrix Multiply (GeMM) Accelerator with Generic Interfaces designed in CHISEL HDL.* *[In Progress]*

Hardware accelerator developed in CHISEL HDL specifically for accelerating Generic Metric Multiply (GeMM) operations and shall be based on a Network on Chip architecture with generic interfaces. (Hardware + Software)

SoC-Now — *A Mini SoC Generator based on Scala and CHISEL. (Final Year Project)*

Developed a Web based SoC Generator which will generate a customized SoC, generate any custom component and verify core and/or SoC. The Generator is completely developed on CHISEL HDL along with the Functional Programming Paradigm of Scala to achieve high level reusability.

SKILLS

Python Programming Language

RISC-V

Scala

Constructing Hardware in Scala Embedded Language (CHISEL) HDL

C language

Bash Scripting

Makefiles

Object Oriented Software Engineering

Embedded Software Programming

FPGA Emulation

Cloud FPGA Emulation (AWS-FPGA)

LANGUAGES

English

Urdu

Chinese (basic)

Google MPW6 — *Participated in MPW6*

Generated a SoC from our SoC-Now SoC Generator and submitted in Google's MPW6 Shuttle Programme for tapeout.

LFX Mentorship— *Porting AOSP 12 Emulator to RISC-V RV64GC*

Selected and Completed in LFX Mentorship programme in a project to port Android 12 Emulator to RISC-V RV64GC Architecture.

The NOVA Project— *Software Team for Cloud FPGA Emulation and Support*

Emulated multiple RTL Designs on AWS-FPGA Cloud FPGA Platform by writing runtime drivers. Configured Zephyr RTOS for the designed RISC-V based SoC and wrote Linux Kernel Device Drivers to boot OS by writing data into DDR.

Reverse Engineering of Rocket Chip — *To Reverse Engineer the Rocket Chip SoC Generator*

Reverse Engineering of the Rocket Chip SoC Generator's Core source code by means of Software Methodologies i.e (Class Diagrams, Flow Charts). Presented in RISC-V Summit 2020

Ababeel Pipelined — *A Risc-V RV32i 5 Stage Pipelined Core*

A Five Stage Pipelined Processor Core based on RISC-V ISA, supporting Integer (i) extension, implemented on CHISEL HCL.

PUBLICATIONS

ChipShop: A Cloud-Based GUI for Accelerating SoC Design

(**RISC-V Summit Europe 2023**)

(**First FireSim and Chipyard Workshop at ASPLOS 2023**)

SoC-Now: An Open-Source Web based RISC-V SoC Generator

(**Workshop on Open Source EDA Technology (WOSET) 2023**)

Bitstream Chef

(**Workshop on Open Source EDA Technology (WOSET) 2023**)

Reverse Engineering of Rocket-Chip

(**RISC-V Summit 2020**)